REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of November 13, 2007 (hereinafter "Office Action"). In response, Applicants have amended Claim 11 to recite "sequentially outputting y-bit comparison result data", as similarly recited in Claim 1. No new matter has been added.

Accordingly, Applicants respectfully request reconsideration of the pending claims for the reasons discussed below.

The Section 112 Rejections

Claims 1, 10, 11, and 21 stand rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement. *See* Office Action, pages 2-3. In particular, the Office Action asserts that the recitations of "comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step are not supported by the specification". Office Action, Page 3.

Applicants respectfully disagree. With regard to the recitations of Claims 1 and 11, Applicants refer the Examiner to Figures 3 and 4 and the corresponding description provided in the present specification. In particular, the nm memory cell arrays are designated by memory cell regions (1) to (8), the x-bit data is designated by each 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12 and ODO13-16) output from each of the nm memory cell arrays (1) to (8), the nm-bit comparison result data is designated by MA1-8 generated by comparing each of the 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12, ODO13-16), and the y-bit data is designated by ma1-4. *See* Specification, Figs. 3-4.

The present specification describes comparing x-bit data output from each of the nm memory cell arrays, for example, at Page 3. Applicants note that, because the description of the function and operation of the comparator 16 is discussed in detail with reference to Figure

1 in the present specification, such description is omitted in the discussion of Figure 3 for the sake of brevity. In particular, the present specification provides that"[t]he comparator 16 compares, by 4 bits, test data [i.e., x-bit data] EDO1~4, EDO5~8, EDO9~12, EDO13~16, ODO1~4, ODO5~8, ODO9~12, and ODO13~16 output from the memory cell regions (1) to (8) [i.e., nm memory cell arrays], respectively, to generate 8-bit comparison result data MA1 to MA8 [i.e., nm-bit comparison data] ..." Specification, Page 3, lines 18-21. Thus, Applicants submit that the recitations of "comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data", as recited by Claims 1 and 11, are fully supported by the present specification.

The present specification also describes sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively. In particular, the present specification notes that "the selecting circuit 20 ... outputs either 4-bit comparison result data MA1 to MA4 or 4-bit comparison result data MA5 to MA8 as 4-bit data ma1 to ma4 in response to a control signal CON." Specification, Page 8, lines 10-13. Applicants submit that the 4-bit comparison result data ma1 to ma4 is y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal. The specification further notes that "[t]he 4-bit data ma1 to ma4 [i.e., the y-bit comparison result data] are output through the 4 data I/O pads DQ1, DQ5, DQ9, and DQ13 [i.e., the y data I/O pads]." Specification, Page 8, lines 13-14. Furthermore, as described at Pages 7-8 of the present specification:

> Referring to FIG. 3, when a control signal is set to a "low" level..., the selecting circuit 20 receives 8-bit comparison result data [i.e., nm-bit comparison result data]...and selects 4-bit comparison result data MA1 to MA4, ..., to output as data ma1 to ma4 [i.e., y-bit comparison result data]. The 4-bit data ma1 to ma4 are then output ... through data I/O pads DQ1, DQ5, DQ9, and DQ13 [i.e., the y data I/O pads]. ... when a control signal CON is set to a "high" level..., the selecting circuit 20 receives 8-bit comparison result data [i.e., nm-bit comparison result data]... and selects 4-bit comparison result data MA5 to MA8, ... , to output as 4-bit data ma1 to ma4 [i.e., y-bit comparison result data]. The 4-bit data ma1 to ma4 are then output...through the data I/O pads [i.e., the y data I/O pads]...

Specification, Page 7, line 30 to Page 8, line 9. Thus, Applicants submit that the recitations of "sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads", as recited by Claims 1 and 11, are also fully supported by the present specification.

With regard to the recitations of Claims 10 and 21, Applicants refer the Examiner to Figures 5 and 6 and the corresponding description provided in the present specification. In particular, the nm memory cell arrays are designated by memory cell regions (1) to (8), the x-bit data are designated by each of the 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12 and ODO13-16) output from each of the nm memory cell arrays (1) to (8), the nm-bit comparison result data are designated by MA1-8 generated by comparing each of the 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12, ODO13-16), and the y-bit data is designated by MAA1-4. *See* Specification, Figs. 5-6.

Applicants submit that the recitations of "comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data" in Claims 10 and 21 are fully supported by the portions of the specification discussed above with reference to Claims 1 and 11.

The present specification also describes grouping and outputting the nm-bit comparison result data into y groups by bit data generated with respect to a control signal. In particular, the present specification provides:

> Referring to FIG. 5, the selecting circuit 24 receives 8-bit comparison result data MA1 to MA8 [i.e., nm-bit comparison result data] ...When a control signal has a "low" level, the selecting circuit 24 selects and outputs, by 2 bits, the comparison result data (MA1, MA5), (MA2, MA6) and (MA3, MA7), (MA4, MA8) [i.e., y groups]...On the other hand, when a control signal CON has a "high" level, the selecting circuit 24 selects and outputs, by 2 bits, the comparison result data (MA1, MA3), (MA2, MA4), (MA5, MA7), and (MA6, MA8) [i.e., y groups]...

Specification, Page 10, lines 12-20. The present specification further describes outputting y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads:

> Still referring to FIG. 5, the comparator 26 outputs first comparison result data MAA1, MAA2, MAA3, and MAA4 [i.e., y-bit comparison result data], which is generated by comparing the 2-bit comparison result data (MA1, MA5), (MA2, MA6) and (MA3, MA7), (MA4, MA8) [i.e., the y grouped bit data] output...to the data I/O pads DQ1, DQ5, DQ9, and DQ13 [i.e., y data I/O pads] when the control signal has a "low" level. Next, the comparator 26 outputs second comparison result data [i.e., y-bit comparison result data]..., which is generated by comparing the 2-bit comparison result data [i.e., the y grouped bit data]..., to the same data I/O pads [i.e., y data I/O pads]...when the control signal is set to a "high" level.

Specification, Page 10, lines 23-31. Thus, Applicants submit that the recitations of "grouping and outputting the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal, and outputting y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads", as recited in Claims 10 and 21, are fully supported by the present specification.

Accordingly, Applicants submit that the present specification as originally filed provides full support for the recitations of Claims 1, 10, 11, and 21. Thus, Applicants respectfully request withdrawal of the rejections of these claims and the claims dependent therefrom under 35 USC section 112, first paragraph, for at least the above reasons.

The Section 102 Rejections

Claims 1-3, 10-13, 21, and 37-41 stand rejected under 35 USC §102(a) as being anticipated by Applicant Admitted Prior Art (U.S. Patent Application Publication No. 2004/0252549; hereinafter "AAPA"). Claim 1, for example, recites:

> 1. A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:
>
> extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step; and
>
> comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and sequentially

> outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. (*Emphasis added*).

Applicants respectfully submit that the AAPA fails to disclose or suggest at least the recitations of the test data read step of Claim 1, as highlighted above.

For example, nowhere does the AAPA disclose or suggest "sequentially outputting the y-bit comparison result data". Rather, as described in the AAPA, "[t]he 8-bit comparison result data MA1 to MA8 [i.e., the nm-bit comparison result data] is output...through the data I/O pads DQ1, DQ3, DQ5, DQ7, DQ9, DQ11, DQ13, and DQ15 [i.e., the nm data I/O pads]." AAPA, Paragraph 0011, lines 34-36. As further described in the AAPA:

> Comparator blocks 32-1 to 32-4 compare the 2-bit comparison result data ...in order to output comparison result data MA1 to MA4...through data I/O pads DQ1, DQ3, DQ5, and DQ7, respectively. The comparators 32-5 to 32-8 compare the 2-bit comparison result data...in order to output comparison result data MA5 to MA8 ... through data I/O pads DQ9, DQ11, DQ13, and DQ15, respectively.

AAPA, paragraph [0013], lines 14-23. As such, the AAPA describes that the comparator blocks 32-1 to 32-8 output 8-bit comparison result data MA1 to MA8 (the nm-bit comparison result data) through 8 data I/O pads DQ1, DQ3, DQ5, DQ7, DQ9, DQ11, DQ13, and DQ15 (the y data I/O pads), respectively. In other words, the AAPA describes that the 8-bit comparison result data is *simultaneously* outputting through 8 data I/O pads, one bit per pad. *See also* AAPA, Fig. 1. Thus, the AAPA does not disclose or suggest *sequentially* outputting the 8-bit data through a different number of data I/O pads (i.e., *y* data I/O pads), for example, the data I/O pads DQ1, DQ5, DQ9, and DQ13. *See* Specification, Fig. 3. The AAPA further acknowledges that, when the 8-bit data (MA1 to MA8) is further compared by 2 bits in order to reduce the number of data I/O pads used for a read operation, the tester may not be able to correctly determine the addresses of defective memory cells. *See* AAPA, Paragraph 0016.

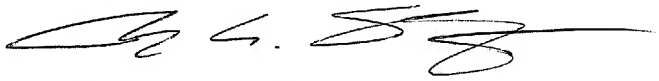
Accordingly, the AAPA fails to disclose or suggest at least the recitations of Claim 1 highlighted above. Thus, Applicants submit that Claim 1 is patentable over the AAPA for at least these reasons. Claim 10 similarly recites "grouping and outputting the nm-bit comparison result data into y groups" and "outputting y-bit comparison result data generated

by respectively comparing the y grouped bit data through the y data I/O pads", and as such, is patentable for at least similar reasons. Claims 11 and 21 include device recitations corresponding to the methods of Claims 1 and 10, respectively, and are thus also patentable for at least similar reasons. Also, dependent Claims 2-3 and 12-13, and 36-41 are patentable at least per the patentability of Claims 1, 10, 11, and 21 from which they depend.

Conclusion

Accordingly, in light of the above amendments and remarks, Applicants respectfully submit that all of the pending claims are now in condition for allowance. Thus, Applicants respectfully request allowance of the pending claims and passing the application to issue. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,



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